Amendments to the Claims

The following Listing of Claims replaces all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1 (currently amended): A common carrier, comprising:

a carrier substrate having an upper surface; and

a plurality of integrated chips distributed across the carrier substrate, each integrated chip including a respective substrate supporting an integrated structure; and

a plurality of adhesive bonds each adhering a respective integrated chip to the carrier substrate;

wherein alignment between the integrated chip substrates is within a first alignment tolerance range and alignment between the integrated structures respectively supported by different [[the]] integrated chip substrates is within a second alignment tolerance range smaller than the first alignment tolerance range.

Claim 2 (previously presented): The common carrier as described in Claim 1, wherein the adhesive bonds comprise an adhesive material selected from polysilicon, glass, metal, and ceramic.

Claim 3 (previously presented): The common carrier as described in Claim 1, wherein the carrier substrate, the adhesive bonds, and the integrated chips have essentially the same coefficient of thermal expansion (CTE).

Claim 4 (previously presented): The common carrier as described in Claim 1, wherein the carrier substrate comprises one of polysilicon, glass, metal, and ceramic.

Claim 5 (previously presented): The common carrier as described in Claim 1, wherein the carrier substrate includes a plurality of slots each containing a respective integrated chip.

Claim 6 (previously presented): The common carrier as described in Claim 5, wherein the upper surface of the carrier substrate and upper surfaces of the integrated chips are substantially coplanar.

Claim 7 (previously presented): The common carrier as described in Claim 6, wherein the upper surface of the carrier substrate and the upper surfaces.

Claim 8 (previously presented): The common carrier as described in Claim 1, wherein the adhesive bonds adhere respective substrates of the integrated chips to the upper surface of the carrier substrate.

Claim 9 (previously presented): The common carrier as described in Claim 8, wherein the integrated structures of the integrated chips are substantially non-coplanar with the upper surface of the carrier substrate.

Claim 10 (previously presented): The common carrier as described in Claim 5, further comprising filler material disposed in each peripheral gap between interior edges of each slot and peripheral edges of each respectively contained integrated chip.

Claim 11 (previously presented): The common carrier as described in Claim 10, wherein the filler material comprises glass frit.

Claim 12 (previously presented): The common carrier as described in Claim 1, wherein the integrated structure of each integrated chip comprises an electrically conductive node, and further comprising an interconnect electrically connecting electrically conductive nodes of the integrated chips.

Claim 13 (previously presented): The common carrier as described in Claim 1, wherein each of the plurality of integrated chips is a component of a respective inkjet printhead.

Claims 14-21 (canceled)

Claim 22 (previously presented): The common carrier as described in Claim 1, wherein the first alignment tolerance range corresponds to a semiconductor chip placement tool alignment tolerance range and the second alignment tolerance range corresponds to a semiconductor lithographic process alignment tolerance range.

Claim 23 (previously presented): The common carrier as described in Claim 1, wherein the first alignment tolerance range is ± 1 millimeter, and the second alignment tolerance range is smaller than 1 micrometer.

Claim 24 (previously presented): The common carrier as described in Claim 5, wherein alignment between the slots of the carrier substrate is within the first alignment tolerance range.

Claim 25 (previously presented): The common carrier as described in Claim 10, wherein the filler material in each gap has a polished upper surface substantially coplanar with the upper surface of the carrier substrate.